COLUMBIA | ENGINEERING
The Fu Foundation School of Engineering and Applied Science

ELEN E3106/4106 Lecture 19

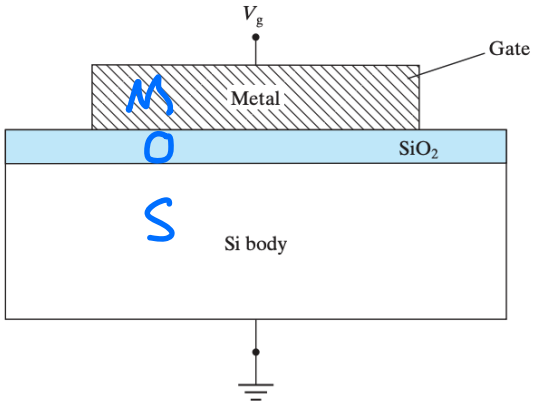
Metal-Oxide-Semiconductor (MOS) Capacitor

Outline

- Basic MOS capacitor theory using n-type (NMOS) device
- Band diagrams for different gate voltage conditions
- Surface potential and depletion width
- Charge densities in the MOS cap

Assignments:
Reading: C. Hu §5.1-5.5
Homework 7 due Fri. Nov. 14th by 5pm

Basic Device Structure and Evolution



- Layer stack:
  - Semiconductor body or substrate
  - Insulator film (ex. SiO_2) also called the dielectric
  - Metal electrode called a gate
- MOS structure is essentially equivalent to a parallel plate capacitor where one plate is a semiconductor
- Evolution of gate with time
  - Before 1970, the gate was made of metal like Al
  - But after 1970, heavily doped polycrystalline (poly) Si has been used instead. Why?

    It can withstand high temps w/o reacting with SiO_2
  - But, the name MOS stuck
  - After 2008, the trend has been to reintroduce metal gates and replace SiO_2 with a high k-dielectrics. More on this later!
- The MOS capacitor is rarely used in itself, but is needed for MOSFETs (transistors)

Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

Flat-Band Condition

- *Flat-band condition* is when E_c, E_v are flat
- What's the gate voltage? $V_G =$ V_{FB}
- Flat-band voltage, V_{FB} = voltage needed on gate to get E-field = 0 everywhere (flat bands)
  - Note, this can be zero ("ideal" MOS), but generally depends on gate Φ_M or doping, $qV_{FB} = q(\Phi_M - \Phi_S)$
- What's the energy barrier seen by e-?

  $3.1\ eV = E_{c,SiO_2} - E_{c,Si}$
- What's the energy barrier seen by h+?

  $4.8\ eV = E_{v,Si} - E_{v,SiO_2}$
- Energy barriers between Si-SiO_2 are large, so carriers cannot easily pass through the gate dielectric
- Does position of E_{F,SiO_2} matter?

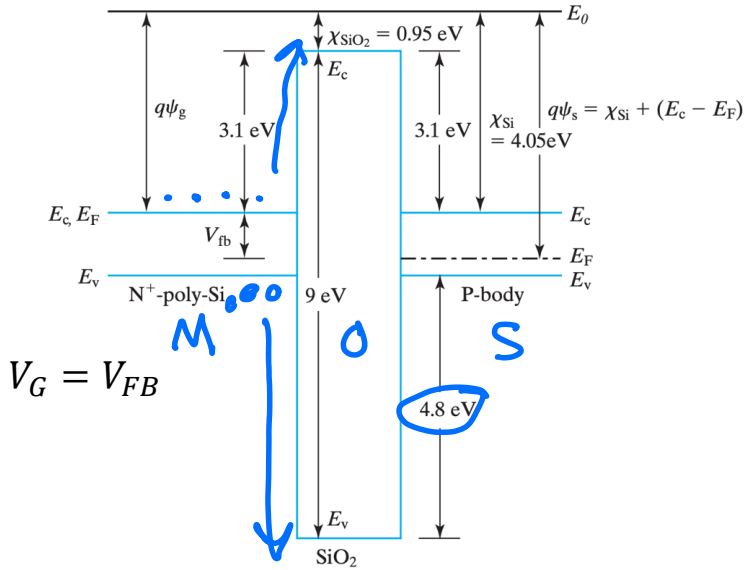
  No, we don't draw it

$n = N_c e^{-\frac{E_c - E_F}{kT}}$

Assume $E_F \approx E_i$

$n \approx 10^{-60}\ cm^{-3}$

Detailed band diagram for n⁺-poly-Si gate, SiO_2 insulator, p-silicon body



Recall:

E_{vac}: Vacuum level

$\chi = E_{vac} - E_C$: Electron affinity

$q\Phi_M = E_{vac} - E_{F,M}$: Metal work function

$q\Phi_S = E_{vac} - E_{F,S}$: Semiconductor work function

Like what we found for the built-in potential, qV_0:

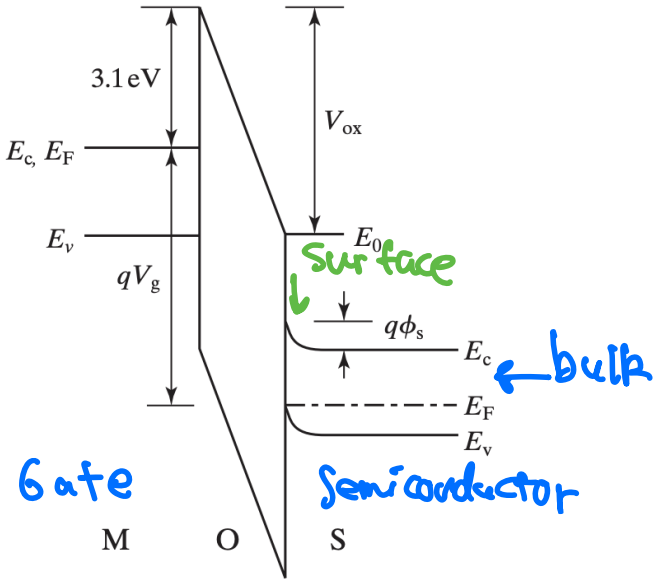
$qV_{FB} = q(\Phi_M - \Phi_S)$: Flat -band potential

*Note: $E_{g,SiO_2} =$ 9 eV

Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

Surface Accumulation

- How does the band diagram change when a more negative gate voltage is applied (e.g. V_g < V_{fb})
- -V_g raises the bands on gate side (recall: (-) voltages raise the bands; (+) voltages lower them)
- When $V_g \neq V_{fb}$, we must introduce 2 additional terms
- ϕ_S, surface potential (units: V). $q\phi_S$ is the degree of band bending in the substrate (units: eV)
  - (-) if $E_{c,S}$ bends upwards towards the surface
  - (+) if $E_{c,S}$ bends downwards towards the surface
- V_{ox}, oxide voltage
  - (-) if the insulator band diagram tilts towards gate
  - (+) if the insulator band diagram tilts away from gate



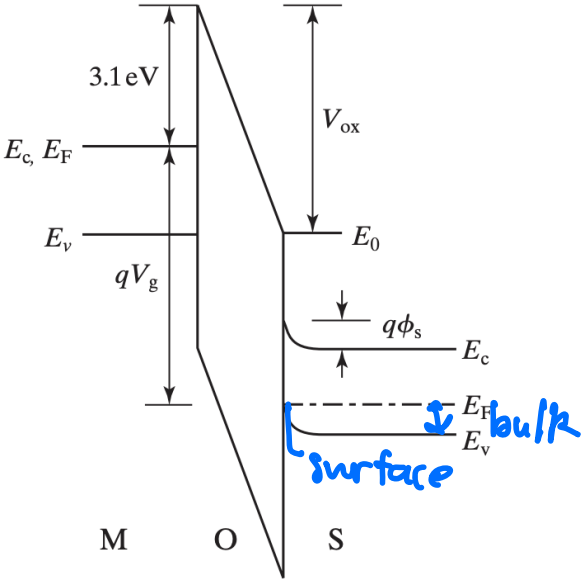
Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

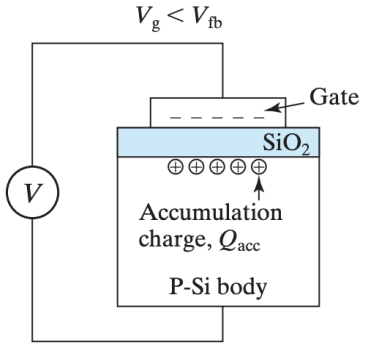
Surface Accumulation

- Notice E_v is closer to E_F at the semiconductor surface than in the bulk (for p-type substrate)
- The semiconductor surface h⁺ concentration, p_s is now larger than the bulk h+ concentration, $p_0 \cong N_A$

$$p_s = N_a e^{-q\phi_s/kT}$$

- The large # of h+ at the surface form an accumulation layer on semi side of O-S interface and the *accumulation charge density* is denoted Q_{acc} (Units: C/cm²)
- If substrate were n-type, there would instead be e^- accumulation
- Typically, $p_s \gg p_0 = N_a$ because $\phi_S \sim -200$ mV





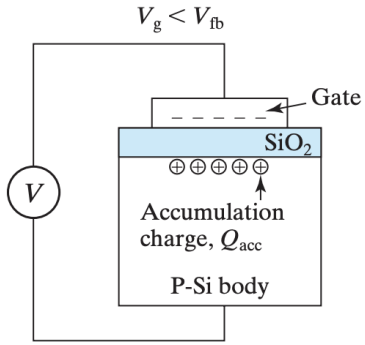
Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

Voltage, Charge, and Capacitance in the MOS

- What's the relationship between the voltages we've discussed so far?

$$V_g = V_{fb} + \phi_s + V_{ox}$$

$\epsilon = \epsilon_r \epsilon_0$



- At flat-band, $V_g = V_{fb}$; $\phi_S = V_{ox} =$ ____
- When $V_g \neq V_{fb}$; ϕ_S *and* V_{ox} must pick up the difference
- Usually, ϕ_S is small and can be ignored, such that

$$V_{ox} = V_g - V_{fb}$$

thickness of oxide layer

- From Gauss's law, $E_{ox} =$ $-\frac{Q_{acc}}{\epsilon_{ox}}$; $V_{ox} =$ $E_{ox} * T_{ox}$; $Q_{acc} = -C_{ox}(V_g - V_{fb})$
- C_{ox}: oxide capacitance per unit area (units: F/cm^2); ϵ_{ox}: oxide permittivity/dielectric constant (units: F/m)
- Why do we have the (-) in the standard $V = Q/C$ capacitor relationship?
  - Usually the cap voltage and charge are taken from the same electrode
  - In MOS, the voltage is the gate volage, but the charge is the substrate charge
- So, the MOS capacitor in accumulation behaves like a cap with Q = C-V but with a shift in V by V_{fb}
- In general, Q_{sub} is all the charge that is present in the substrate, including Q_{acc} and we can more generally write:

$$V_{ox} = -Q_{sub}/C_{ox}$$

Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

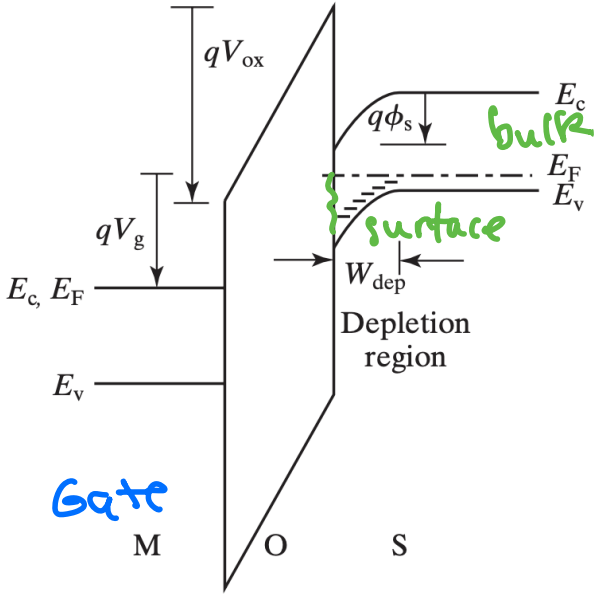
Depletion

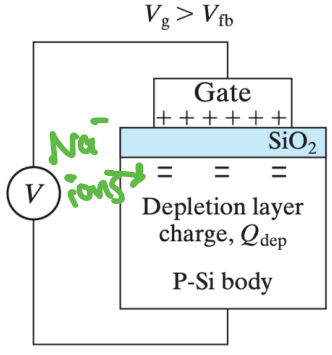
- How does the band diagram change when a more *positive* gate voltage is applied (e.g. V_g > V_{fb})?
- $+V_g$ (relative to V_{fb}) lower bands on gate side (recall: (-) voltages raise the bands; (+) voltages lower them)
- This is the opposite case of accumulation. Now we have a semiconductor surface that is depleted of carriers
  - E_v is *further from* E_F at the semiconductor surface than in the bulk
- W_{dep} is the depletion region width, and our relevant equations are:

$$W_{dep} = \sqrt{(2\varepsilon_s \phi_s)/(qN_a)} \qquad \phi_s = \frac{qN_a W_{dep}^2}{2\varepsilon_s} \qquad V_{ox} = -\frac{Q_{sub}}{C_{ox}} = -\frac{Q_{dep}}{C_{ox}} = \frac{qN_a W_{dep}}{C_{ox}} = \frac{\sqrt{qN_a 2\varepsilon_s \phi_s}}{C_{ox}}$$

- Why is Q_{dep} negative? Only uncompensated ions (N_a^-) are left behind
- So, now we can solve for W_{dep} as a function of V_g. With W_{dep}, we can find ϕ_s and V_{ox}

$$V_g = V_{fb} + \phi_s + V_{ox} = V_{fb} + \frac{qN_a W_{dep}^2}{2\varepsilon_s} + \frac{qN_a W_{dep}}{C_{ox}}$$





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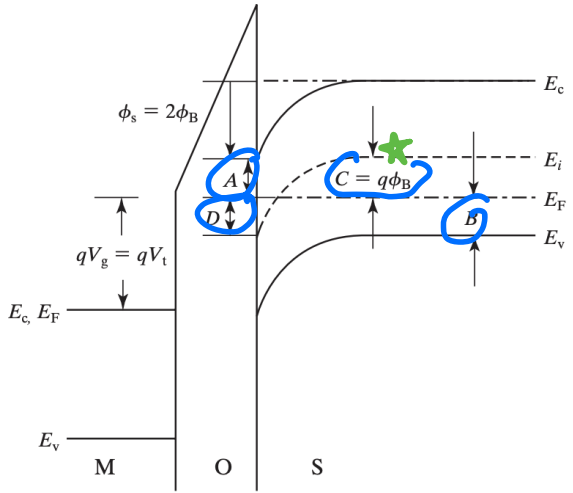
Threshold Condition

- What happens are we make the gate voltage increasingly more positive (e.g. $V_g > V_{g,acc} > V_{fb}$)?
- $+V_g$ bends the bands down (dep) even further
- At some V_g, the surface will no longer remain in depletion but instead enter the threshold of inversion
- *Inversion*: when the surface is inverted from p-type to n-type (e.g. $E_F, surface > E_i$) *or vice versa*
- What is the condition for inversion?
- Therefore, A = B and C = D in our diagram
- Note: Bulk potential, denoted ϕ_F in Streetman, = $\Phi_B = \frac{1}{q}[E_i(bulk) - E_F]$
- ϕ_{st} is the surface potential (band bending) at threshold
- V_t is the threshold voltage, the gate voltage at which the surface changes from depletion to inversion
  - Function of the Tox and substrate/bulk doping



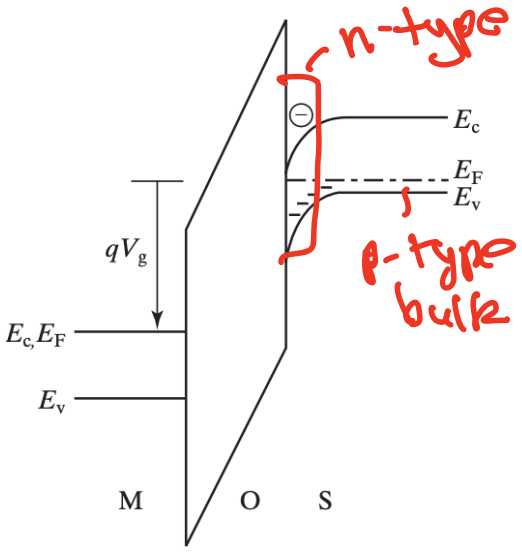
$$\phi_{st} = 2\phi_B = 2\frac{kT}{q}\ln\frac{N_a}{n_i}$$

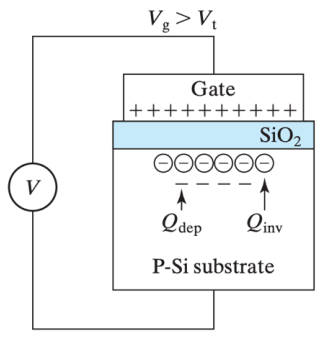
$$V_t = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{C_{ox}}$$

Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

Inversion

- As we increase the gate voltage past the threshold voltage (e.g. $V_g > V_t$), we induce strong inversion in the MOS cap
- Now we have an *inversion layer* of e^- (p-type body), with an inversion charge density Q_{inv} (units: C/cm^2)
- Where do they come from? Thermally generated
- We can visualize this as a very thin n-type layer at the p-type semiconductor surface
- Past threshold, all additional charge gets put on the gate, which is mirrored by the charge in the inversion layer
- ϕ_s will not increase much past threshold $\phi_{st} = 2\phi_B$, because the inversion layer e- do not affect the E-field in semiconductor





Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

Inversion

- If ϕ_s doesn't increase, W_{dep} has reached its maximum, W_{dmax}

$$W_{\mathrm{dmax}} = \sqrt{\frac{2\varepsilon_s 2\phi_B}{qN_a}}$$

- Now, our gate voltage is:

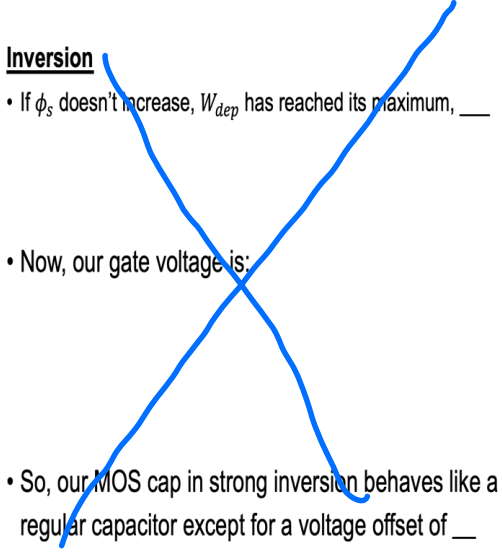
$$V_g = V_{fb} + \phi_s + V_{ox}$$

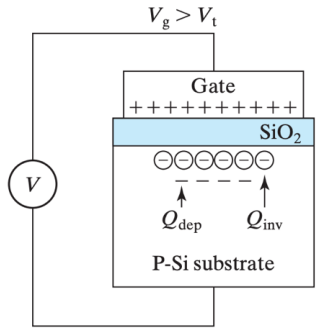
$$V_g = V_{fb} + 2\phi_B - \frac{Q_{dep}}{C_{ox}} - \frac{Q_{inv}}{C_{ox}} = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\varepsilon_s 2\phi_B}}{C_{ox}} - \frac{Q_{inv}}{C_{ox}}$$

$$= V_t - \frac{Q_{inv}}{C_{ox}}$$

$$\therefore \quad Q_{inv} = -C_{ox}(V_g - V_t)$$

- So, our MOS cap in strong inversion behaves like a regular capacitor except for a voltage offset of V_t





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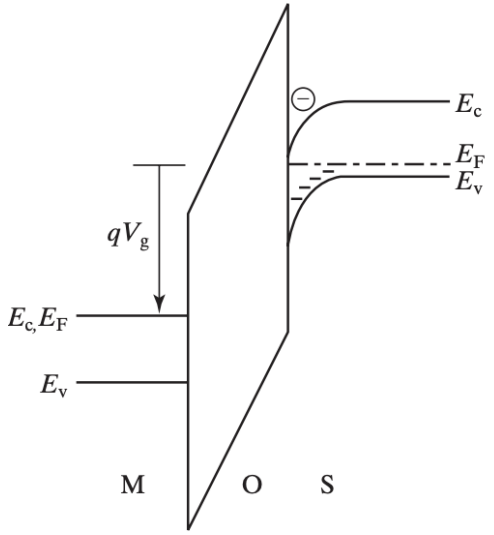
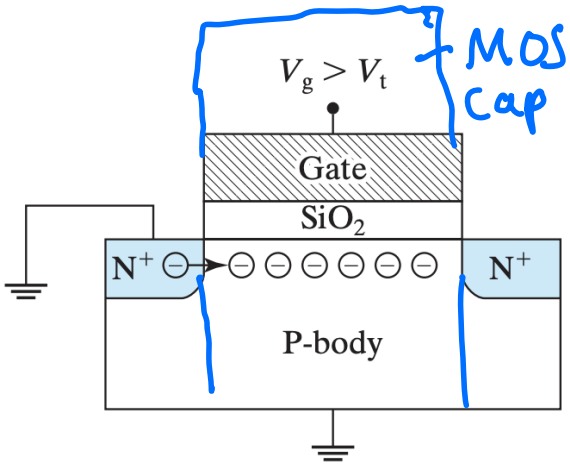
Preview of MOSFET

- We have assumed that e- appear in the inversion layer when E_F approaches E_c at the surface
- But, there aren't many e- available in the p-type body
- It can take minutes to thermally generate e- to form inversion layer
  - Slow !
- How do we solve this problem?
- Use a metal-oxide-semiconductor (MOS) field-effect transistor (FET)
- Inversion layer e- are supplied by the n^+ wells on either side of the MOS cap

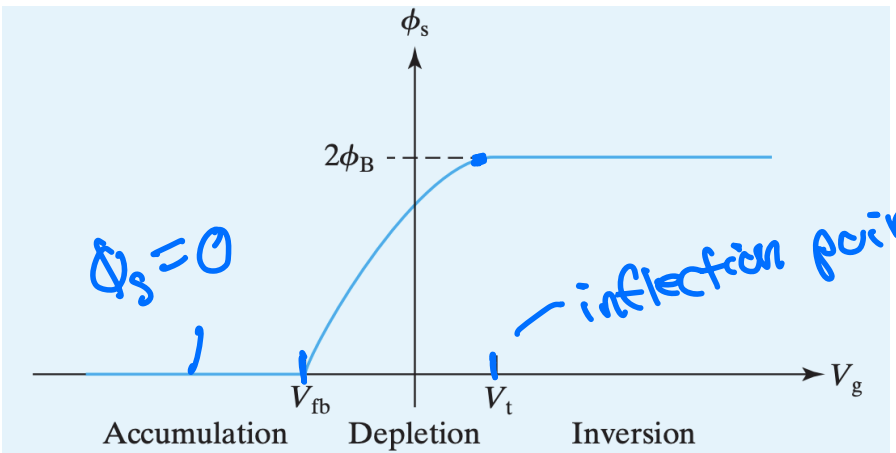




Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

Summary: Surface Potential Versus Gate Voltage

- $\phi_s = 0$ at $V_g = V_{fb}$ and in accumulation
- ϕ_s increases from zero towards $2\phi_B$ in depletion
- When $\phi_s = 2\phi_B$, the surface e- concentration becomes so large the surface is considered inversion to n-type
  - The V_g at this point is called the threshold voltage, V_t
- The surface potential saturates at $2\phi_B$



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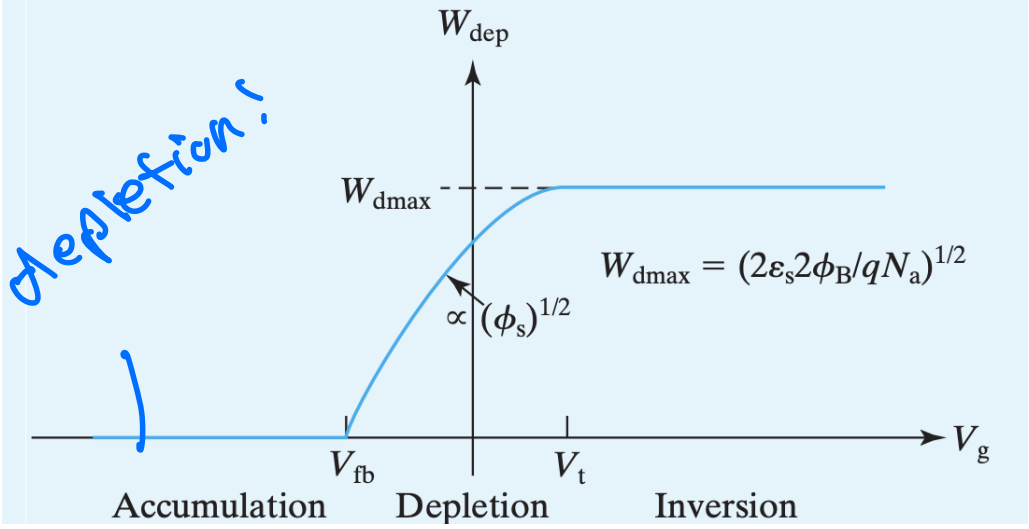
Summary: Depletion Width Versus Gate Voltage

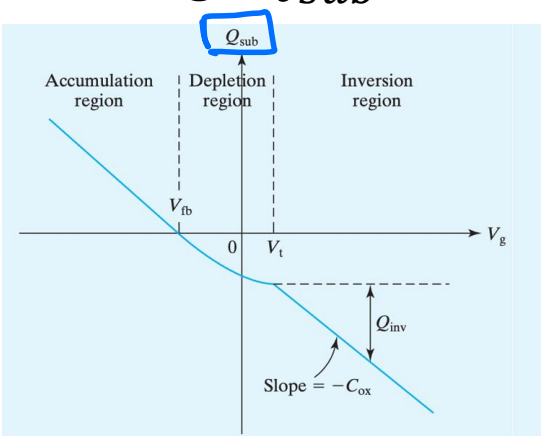
- No depletion region when MOS is in accumulation
- We apply the depletion approximation we used for p-n diodes ($W_{dep} \propto \sqrt{V}$)
- W_{dep} saturates when $V_g \geq V_t$ because surface potential saturates at $2\phi_B$

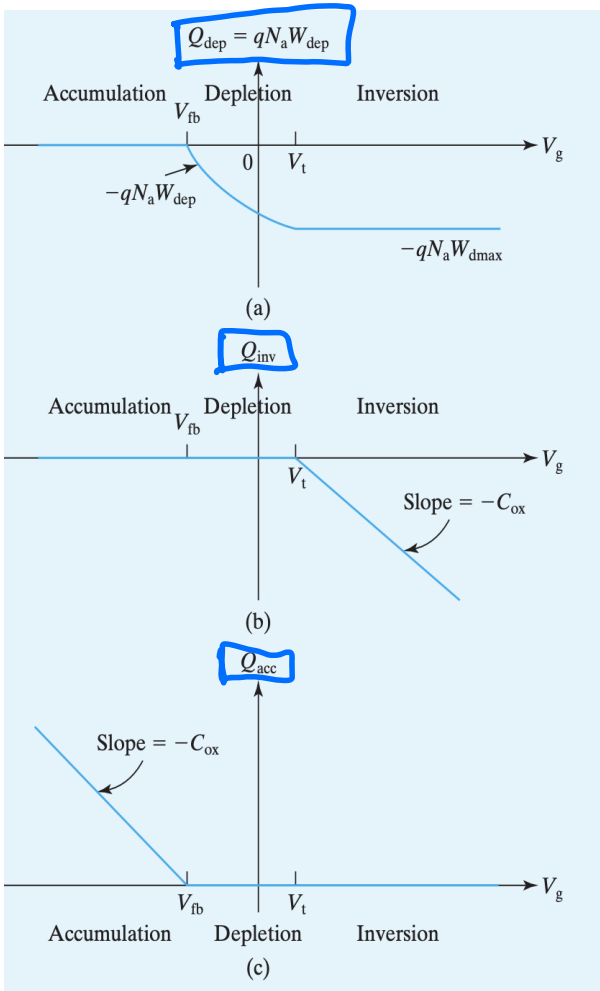


Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

Summary: Charge Components Versus Gate Voltage

- We discussed 3 charge components: $Q_{dep}, Q_{inv}, Q_{acc}$
- Q_{dep} is constant in inversion since W_{dep} is constant
- In inversion, $Q_{inv} = -C_{ox}(V_g - V_t)$ appears
- In accumulation, $Q_{acc} = -C_{ox}(V_g - V_{fb})$ appears
- The slope is $-C_{ox}$ in acc. and inv. Regions
- The total substrate charge Q_{sub} is the sum of the 3 components

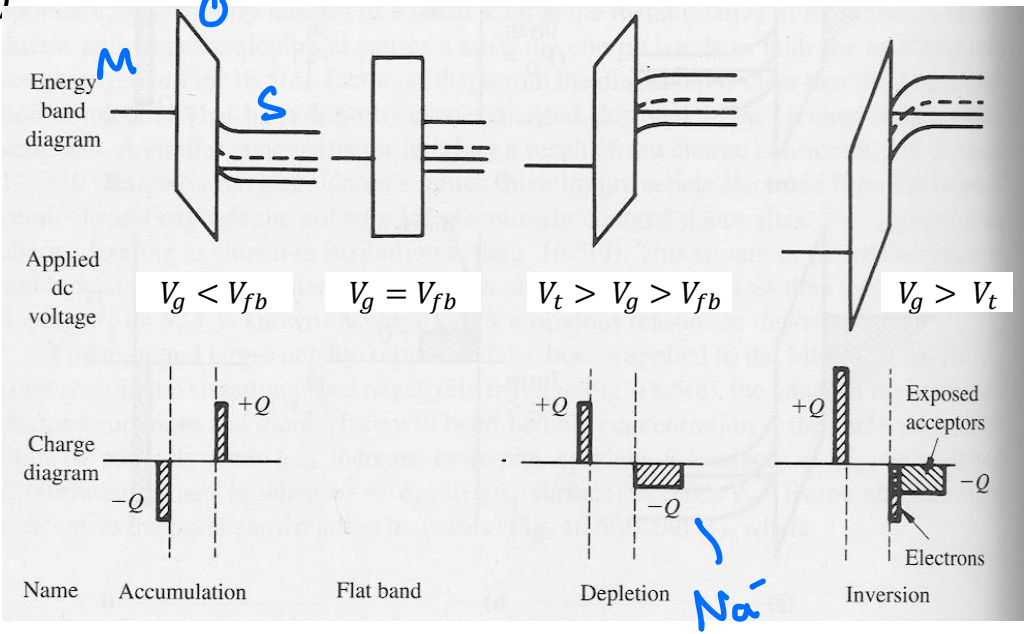




Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*

Summary: Band Diagrams and Charge Diagrams for Bias Conditions

- The band diagrams for 4 different gate voltage bias conditions are shown below (threshold not shown)
  - Accumulation
  - Flat-band
  - Depletion
  - Inversion
- Note that these diagrams are for an n-type MOS cap which we have been discussing today
  - n^+-poly gate over p-type substrate
- The "type" refers to the type of _____
- As we've seen with every other device type, there's an equivalent p-type MOS cap
  - p^+-poly gate over n-type substrate



Sources: E. Pop ECE 340 Lecture Slides